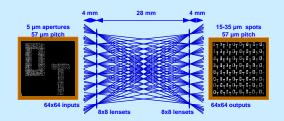


VLSI PHOTONICS



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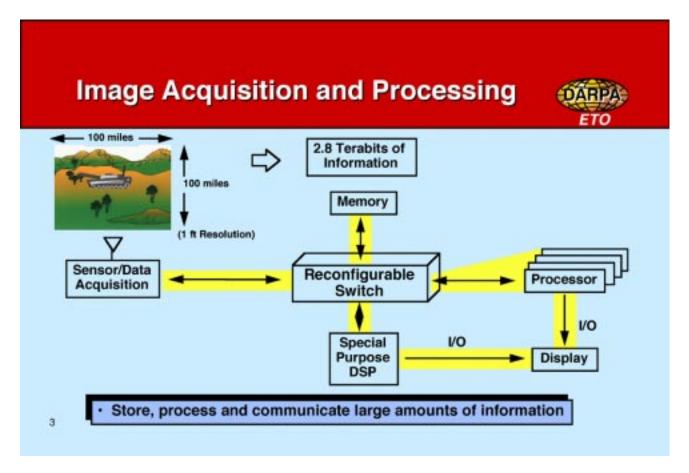
Outline



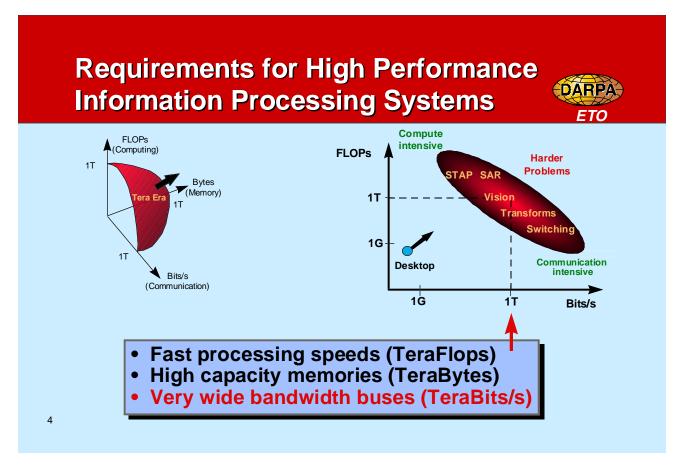
- Introduction
- System Hardware Design Considerations
 - Bandwidth
 - Memory Capacity
 - FLOPS
- VLSI Photonics
- Optical Interconnects
 - Key Element (VCSEL)
- Optical Memories
- Heterogenous Integration Technologies
- Applications

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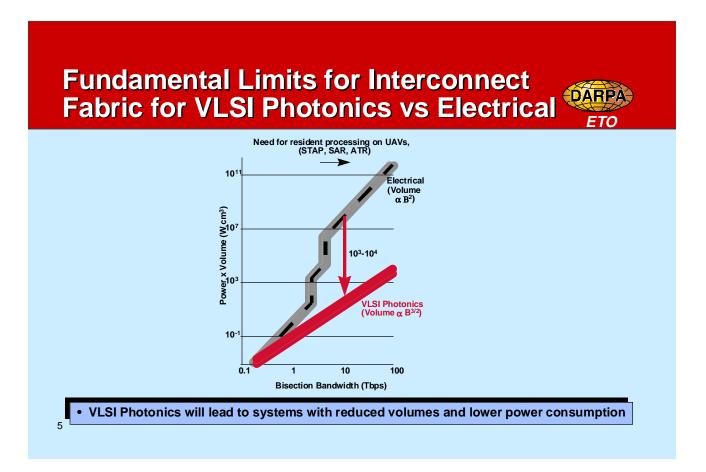
In the information processing systems of the future, the hardware design considerations are going to revolve around three key issues: (i) bandwidth, (ii) memory, and (iii) the processing speed of the system. These systems are going to require large bandwidths and large capacity memories, in addition to fast-processing speeds. Current systems are limited in their ability to achieve these goals because of some of the technologies used. The electrical interconnection technology used, for example, in the backplane interconnection of boards is becoming unwieldy. Interconnections between chips and MCMs are also becoming a problem. These electrical interconnection limitations can be overcome by using optics. The VLSI Photonics Program will take advantage of new developments in large scale integration of optoelectronic devices and VLSI electronics to design interconnection fabrics that overcome most of these problems. The key technology breakthrough that will make optical interconnection fabrics possible is the low threshold current vertical-cavity surface-emitting laser (VCSEL). The memory capacities of these systems will also be increased by using multilayered or volumetric optical memory concepts. Since the optical and electronic devices of VLSI Photonics are not fabricated from the same materials, they must be integrated together using heterogeneous integration techniques. The successful integration of these systems will enable new capabilities and concepts. Some of the applications that are anticipated to benefit from the new capabilities include real-time dynamic target recognition, interactive medical image processing, and virtual reality interactions.



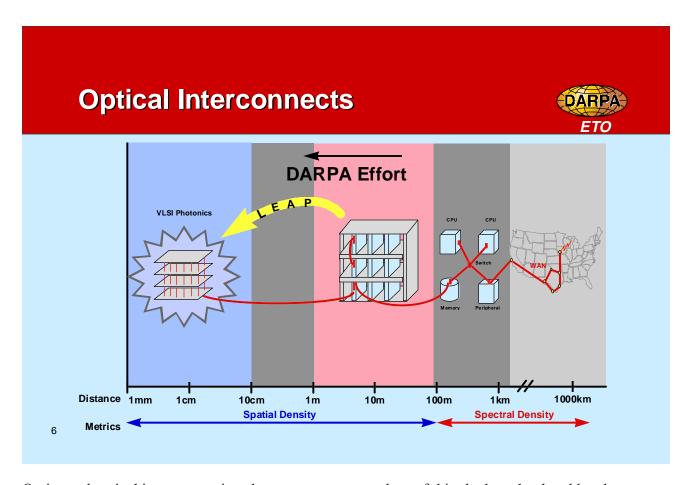
Consider, for example, that we want to image a land area of about 10,000 square miles. This size area will generate about 2.8 Terabits of information (for a 1 foot image resolution). The requirements on the system are very clear: it must store, process and communicate large amounts of information.



The considerations that will define the hardware design issues of next generation information processing systems will be formulated in terms of performance specifications. The most important of these specifications are (i) bandwidth, (ii) memory, (iii) processing speed, (iv) power consumption, and (v) physical size.



The performance specifications I have just outlined imply a high degree of connectivity, which means lots of wires and metal lines. The penalty for this is bulkier systems, slower processing speeds, and high power dissipation. If optical interconnection fabrics are used, however, the power*volume product can be minimized and the speed increased. A comparison of how the bisection bandwidth scales as a function of the power*volume product for both electrical and optical interconnections is shown on this chart. The rationale for the optical interconnection fabrics is clear.



Optics and optical interconnections have proven extremely useful in the long-haul and local area communication networks. The next arena where optics will make an even greater impact will be "in the box" where optics has the potential to solve the electrical interconnect problem at the backplane of boards, between the chips that populate the boards, and between MCMs. At this level of hierarchy, the optical interconnections are spatially dense; this is to be contrasted from the interconnections in the long-haul and local area networks, where they are spectrally dense.

VLSI Photonics



Objective:

Develop novel optoelectronics hardware solutions that maximize **speed/(power*volume)** of large data array processing and communication systems e.g.:

- 2-D fast-frame 1024x1024 complex FFT engine
- Multiprocessor Crossbar Switch

Approach:

Components: VCSEL arrays: >32x32, low threshold

More scaleable receivers

Packaging: Heterogeneous integration, Heat removal

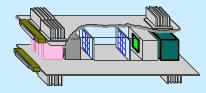
Low cost, reliable alignment procedures

System: Demonstrate system level feasibility

and superiority of optoelectronic

interconnects

Modularity: One suite of easily integrable modules



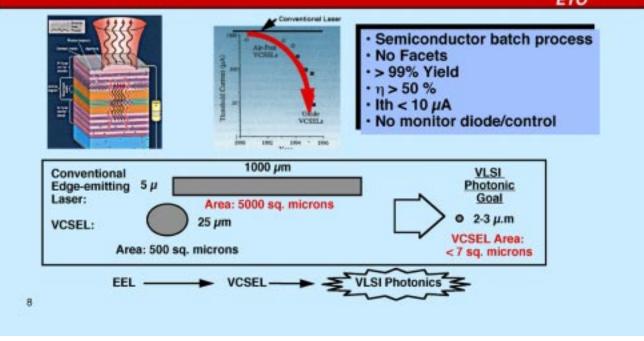
Multidisciplinary Effort:

- Architecture and Applications
 - Design and Optimization
 - Modeling and Simulation
- VCSELs and Detectors
- VLSI Electronics
- Optics
- Components Packaging
- System Packaging
- Demonstrators

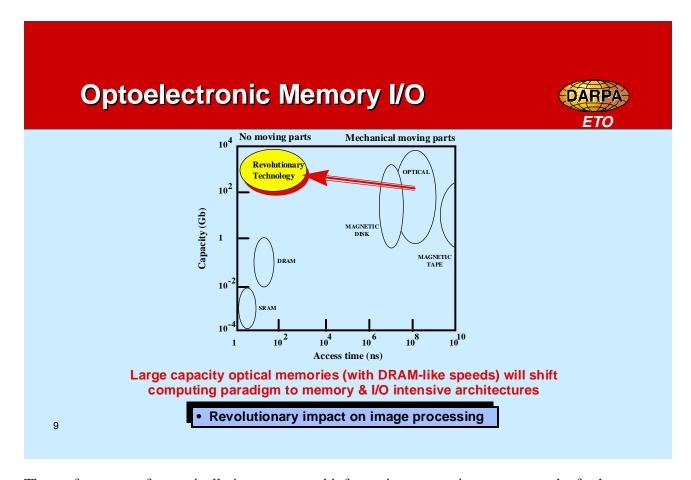
The objectives of the VLSI Photonics Program are to develop innovative optoelectronic hardware solutions to the problems just discussed. These solutions will maximize the speed/(power*volume). They will be developed in a multidisciplinary environment where system integration, architecture considerations, component development and packaging are addressed concurrently.

VCSEL Breakthrough Key Enabler VLSI Photonics

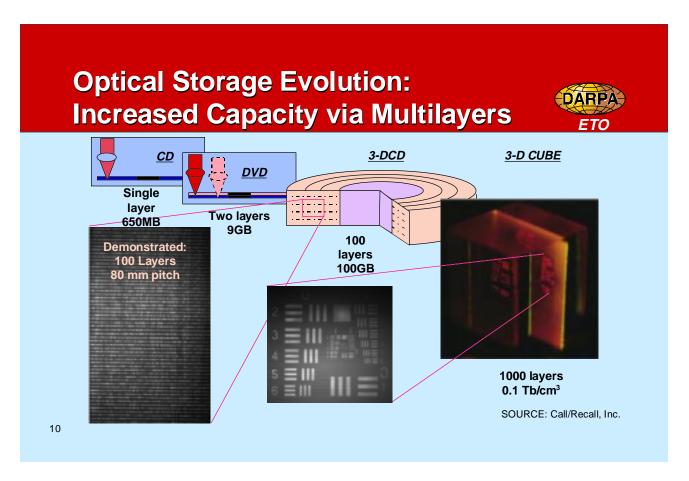




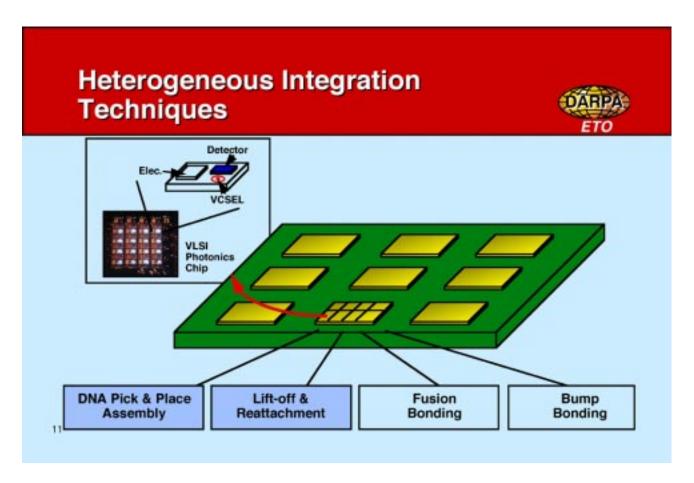
The key enabling technology for the VLSI Photonics Program is the vertical-cavity surface-emitting laser. This device, whose cavity length is only about 6 microns, has a nominal lateral extent of about 3 microns. The cavity mirrors are monolithically formed during the growth of the other layers of the device. Once grown, the VCSEL can be fabricated into linear or two-dimensional arrays in only a few steps using standard microelectronics processing techniques. Lasing threshold currents substantially below a milliampere have been demonstrated, with differential quantum efficiencies of over 50%.



The performance of an optically interconnected information processing system can be further enhanced by including high density optical storage. When accessed in parallel, the optical memory is fully compatible with the interconnection fabrics discussed earlier. The optical memory technologies that will be explored in this program include, but are not limited to, multilayered and volumetric memory technologies. Storage capacities in the 100s of Gbytes are thought to be possible; the raw transfer rates of these memories will easily approach the 100 Gbits/sec range.



Optical storage has evolved from the single layer compact disc to the current digital video disc. The next generation technologies will involve multilayered structures that will be capable of storing 100s of Gbytes. These discs will further evolve into three-dimensional cubes with anticipated storage densities of as high as 1 terabit/cm³.



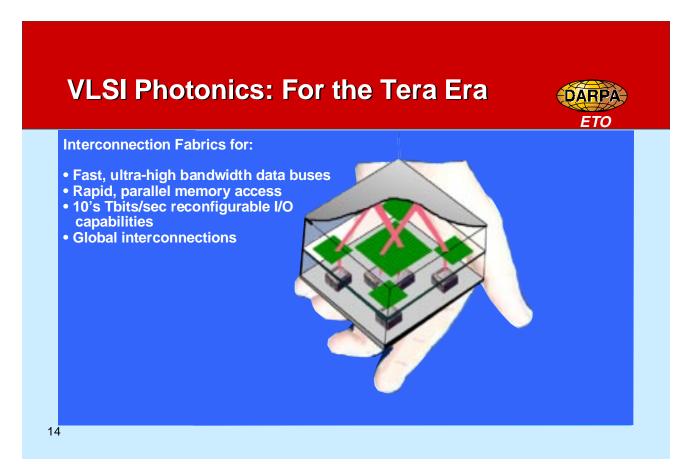
Some of the heterogeneous integration technologies necessary for the interconnect fabrics include flip-chip bonding, wafer fusion, and pick-and-place assembly.

Integration Technologies for VLSI Photonics ETO Lift-off **VCSELs GaAs** Wafer Lift-off and Reattachment 1. Fabricate VCSELs Fabricate VCSELs on GaAs **VCSELs** Lift-off VCSELS from GaAs **GaAs Substrate** substrate 2. Lift-off VCSELs Remount VCSELs on Si from GaAs Substrate **VCSELs Substrate** Host Subs. 3. Mount onto Si Substrate We can now attach GaAs circuitry onto Si wafers 12

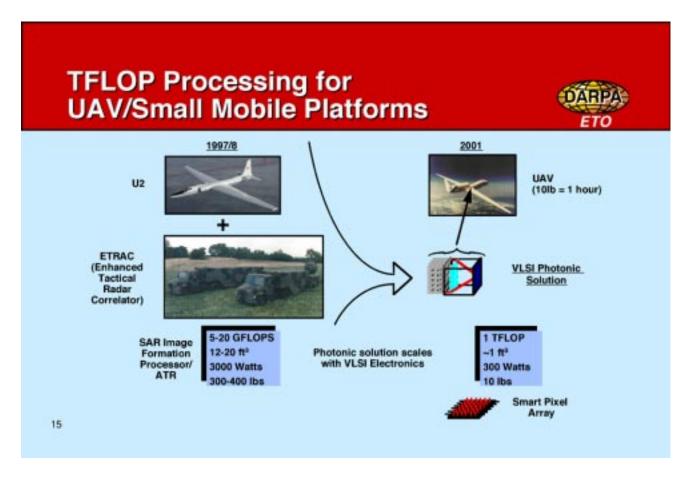
Since the VCSELs can be processed using standard batch processing techniques, we can use lift-off and re-attachment methods to integrate them with the driving Si-based electronics.

A Suite of Applications Using One Set of Technologies Special Purpose Accelerators Special Purpose Accelerators Globally Connected Parallel Processors

The VLSI Photonics interconnection fabrics will enable the design of fast, ultrahigh bandwidth data buses. These buses will be necessary for rapid parallel access to large capacity optical memories.



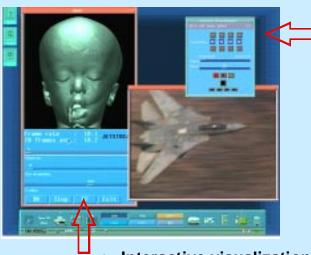
With TeraFlop/s processing capability, it will be possible to design small mobile platforms that are dynamically tasked in real-time. Such platforms include small UAVs with advanced sensors (e.g., SAR).



This technology will have a significant impact on both military and civilian image processing applications.

Real-Time Image Processing Applications





Fast real time data base searches

Interactive visualization in medical image processing

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Two key examples are dynamic target recognition in the battlefield and real-time interactive visualization of medical images (e.g., CAT scans).

Summary



• Impact

- Implement real-time SAR processing
- ATR processors with fast object recognition/correlation
- Interactive battlefield visualization using dynamic databases
- Interactive visualization in medical imaging

New Capabilities

- Reduction of power*volume product for high performance processors
- Fast reconfigurable interconnectivity for multiprocessor systems
- Tbit optical memories with 100's Gbit/s transfer rates (optical ROM with DRAM-like speeds...10's of nanoseconds)
- Key Technologies
 - Low threshold VCSEL
 - Heterogeneous integration technologies

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